

REMARKS

Claims 1-31 are pending in the application and stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,042,687 to Singh et al. (“Singh”) in view of U.S. Patent No. 6,046,116 to DeOrnellas et al. (“DeOrnellas”) and further in view of U.S. Patent No. 5,827,437 to Yang (“Yang”).

By this amendment, claims 1, 14 and 23 have been amended and a marked up version illustrating the claim amendments is annexed hereto. Applicants respectfully request reconsideration of the claim rejections based on the following remarks.

In general, claims 1, 14 and 23 are directed to methods for *etching deep trenches in a silicon substrate*. The etching is performed using reactive plasma at a high wafer temperature of greater than 200 degrees Celsius. The method enables the formation of *deep trenches having a depth of about 7um or greater*. Advantageously, the methods of claims 1, 14 and 23 enable the formation of deep trenches (DT) having depths that are not obtainable using conventional DT etching methods due to the accumulation and re-deposition of etch -by products that cause, e.g., trench “pinch-off”, especially for small ground rule designs.

To establish a *prima facie* case of obviousness, various criteria must be met. For instance, there must be some suggestion or motivation in the references or in the knowledge generally available to one skilled in the art to combine the reference teachings. In addition, the prior art references must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination must both be found in the prior art and not based on applicant’s disclosure (see, e.g., MPEP 2141, 2143, 2143.03). It is respectfully submitted that at the very minimum, the combination of Singh, DeOrnellas, and Yang is legally deficient to establish a *prima facie* case of obviousness for claims 1, 14 and 23.

For instance, it is respectfully submitted that the combination of Singh, DeOrnellas and Yang does not teach or suggest method for forming *deep trenches in a silicon substrate by heating a wafer at high temperatures during a plasma etch*, much less a method for *forming deep trenches in a silicon substrate, wherein the deep trenches have a depth of about 7um or greater*, as essentially claimed in claims 1, 14 and 23

Indeed, although Singh discloses a plasma processing apparatus and a method of use thereof, there is simply nothing in Singh that remotely discloses or suggests an etching method for forming deep trenches in a silicon substrate having depths of about 7um or greater.

Further, although DeOrnellas arguably discloses maintaining the wafer at a high temperature during an etch process, there is nothing in DeOrnellas that discloses or suggests an etching method for forming *deep trenches in a silicon substrate, wherein the trench depths are about 7um or greater*. Indeed, DeOrnellas is directed to method for minimizing the CD (critical dimension) growth of *a feature on the wafer* (e.g., platinum features (or other metals) on the wafer (see, e.g., Col. 5, lines 1-21)). But DeOrnellas does not teach a DT etching method for forming DTs having a depth of *7um or greater*.

Moreover, although Yang arguably discloses a plasma reactor and forming trenches (Fig. 1b), Yang only discloses a method for forming trenches in a *layer stack comprising metallization layers* (see, e.g., Col. 3. lines 29-40. There is nothing in Yang that discloses or suggests an etching method for forming *deep trenches in a silicon substrate, wherein the trench depths are about 7um or greater*. In fact, as clearly shown in Fig. 1, *no* trenches are formed in silicon substrate 102.

Therefore, even if Singh, DeOrnellas and Yang were combinable, the combination would not disclose or suggest the elements of forming *deep trenches in a silicon substrate having*

trench depths of 7um or greater, as essentially claimed in claims 1, 14 and 23. Thus, such combination is legally deficient.

Although it is acknowledged on page 4 of the Office Action that neither Singh, DeOrnellas nor Yang teaches a method for forming deep trenches, it is contended that because Singh, DeOrnellas nor Yang teach the same process steps that “are performed as in the claimed invention, it is inherent that deep trenches are etched in a substrate.” It is respectfully submitted that this conclusion is nothing more than impermissible hindsight based on Applicants’ disclosure, which is improper to sustain an obviousness rejection.

Indeed, as demonstrated above and as acknowledged in the Office Action, none of the cited references discloses forming deep trenches in a substrate. One of ordinary skill in the art would find no motivation in the teachings of Singh (which merely discloses an etching apparatus), DeOrnellas (which teaches etching features (e.g., metallic features) formed on wafer) and Yang (which discloses etching metallization layers on the wafer), to combine such teachings to derive a method for etching a *silicon substrate to form deep trenches having depths of about 7um and greater*, as essentially claimed in claims 1, 14 and 23. Indeed, it is inherent that methods for etching metallic layers on the substrate surface (as disclosed in DeOrnellas and Yang) require different environments (pressure, temperature, etching gases) and parameters than those used for etching a silicon substrate to form deep trenches therein.

Thus, for at least the above reasons, claims 1, 14 and 23 are believed to be non-obvious and patentable over the combination of Singh, DeOrnellas and Yang. Further, all pending claims that depend from claims 1, 14 or 23 are believed to be non-obvious and patentable over such combination *at least* for the reasons given above for respective base claims 1, 14 and 23.

Accordingly, the withdrawal of the all the rejections is respectfully requested.

Respectfully submitted,



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MARKED-UP VERSION ILLUSTRATING CLAIM AMENDMENTS

1. (Twice Amended) A method for etching deep trenches in a substrate, comprising the steps of:

securing a wafer to an electrode in a plasma chamber, the wafer comprising a silicon substrate;

heating the wafer to a temperature of greater than 200 degrees Celsius; and

exposing the wafer to a reactive plasma to etch deep trenches into the silicon substrate of the wafer, wherein the deep trenches have a depth of about 7um or greater.

14. (Twice Amended) A method for etching deep trenches in a substrate, comprising the steps of;

forming a hardmask on a silicon substrate of a wafer;

patterning the hardmask;

securing the wafer to an electrode in a plasma chamber;

maintaining the electrode at a temperature of between about 200 and about 450 degrees Celsius to achieve about the same temperature in the wafer; and

exposing the wafer to a reactive plasma to etch deep trenches into the silicon substrate of the wafer in accordance with the hardmask pattern, wherein the deep trenches have a depth of about 7um or greater.

23. (Twice Amended) A method for etching deep trenches in a substrate, comprising the steps of:

clamping a wafer onto a electrode in a plasma chamber, the wafer comprising a silicon substrate;

maintaining the electrode at an elevated temperature between of about 200 degrees and 450 degrees Celsius;

exposing the wafer to a reactive plasma including Cl₂, BCL₃, Ar, O₂, and N₂;

applying a backside pressure to the clamped wafer using He to achieve thermal contact between the wafer and the electrode such that the wafer is maintained at about the same temperature as the electrode; and

applying a bias power to the wafer electrode to accelerate ions from the plasma to achieve etching of the silicon substrate to form deep trenches, wherein the deep trenches have a depth of about 7um or greater.